AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microcomputer including a read-only memory that stores programs, a controller/calculator that successively accesses addresses of the programs stored in said read-only memory to retrieve and decode an instruction from each of the accessed addresses, to execute a process based on the decoded instruction, and a program counter in which an address to be accessed by the controller/calculator is successively renewed, said microcomputer comprising:

at least one comparison-address-storage device that stores ~~a~~ comparison address data corresponding to an optional address of the programs stored in the read-only memory, at which an interruption-process is executed to virtually revise the programs stored in the read-only memory;

a random-access memory that stores a revisional program in which the interruption-process is ~~programed~~ programmed;

at least one vector-address-storage device that stores vector address data corresponding to a head address of the revisional program stored in said random-access memory;

an address comparator that compares the comparison address data with an address successively renewed in the program counter;

wherein the controller/calculator accesses the head address of the revisional program, stored in said random-access memory, corresponding to the vector address data

stored in said vector-address-storage device, when there is a coincidence between the comparison address data and the renewed address of the program counter, resulting in an execution of the interruption-process in accordance with the revisional program;

a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of the interruption-process in accordance with the revisional program is completed; and

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an address-coincidence-disabling system that disables the coincidence between the comparison address data and the return-address set in the program counter by said return-address-setter.

2. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, further comprising:

a discrimination system that discriminates whether the coincidence between the comparison address data and the renewed address of said program counter is proper; and

the ~~an~~ address-coincidence-disabling system further ~~that~~ disables the coincidence between the comparison address data and the renewed address of the program counter.

3. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, further comprising:

a rewritable and non-volatile memory that stores said revisional program, the comparison address data and said vector address data; and

a reading/writing system that reads the revisional program, the comparison address data and the vector address data from said rewritable and non-volatile memory, and writes the revisional program, the comparison address data and the vector address data in

said random-access memory, said comparison-address-storage device and said vector-address-storage device, respectively, whenever the microcomputer is powered ON.

4. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, wherein said address comparator is connected to the program counter to retrieve the renewed address.

5. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, wherein said address comparator is connected to an address bus extending to the program counter, to retrieve the renewed address from the program counter.

6. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, further comprising a vector-address data setting system that reads the vector address data from said vector-address-storage device, and sets the rector-address-data in the program counter, enabling access to the head address of the revisional program by said controller/calculator, and execution of the interruption-process in accordance with the revisional program.

7. (Currently Amended) The ~~A~~ microcomputer as set forth in claim 1, further comprising:

a vector-address-temporary-storage device that receives the vector address data from said vector-address-storage device, when said address comparator determines that there is coincidence between the comparison address data and the renewed address of the program counter; and

a vector-address data setting system that reads the vector address data from said vector-address-temporary-storage device, and sets the rector-address-data in the program

counter, enabling the access to the head address of the revisional program by said controller/calculator and execution of the interruption process in accordance with the revisional program.

Claim 8 (canceled)